

SL2610 CORE MODULE Schematic

Block Diagram

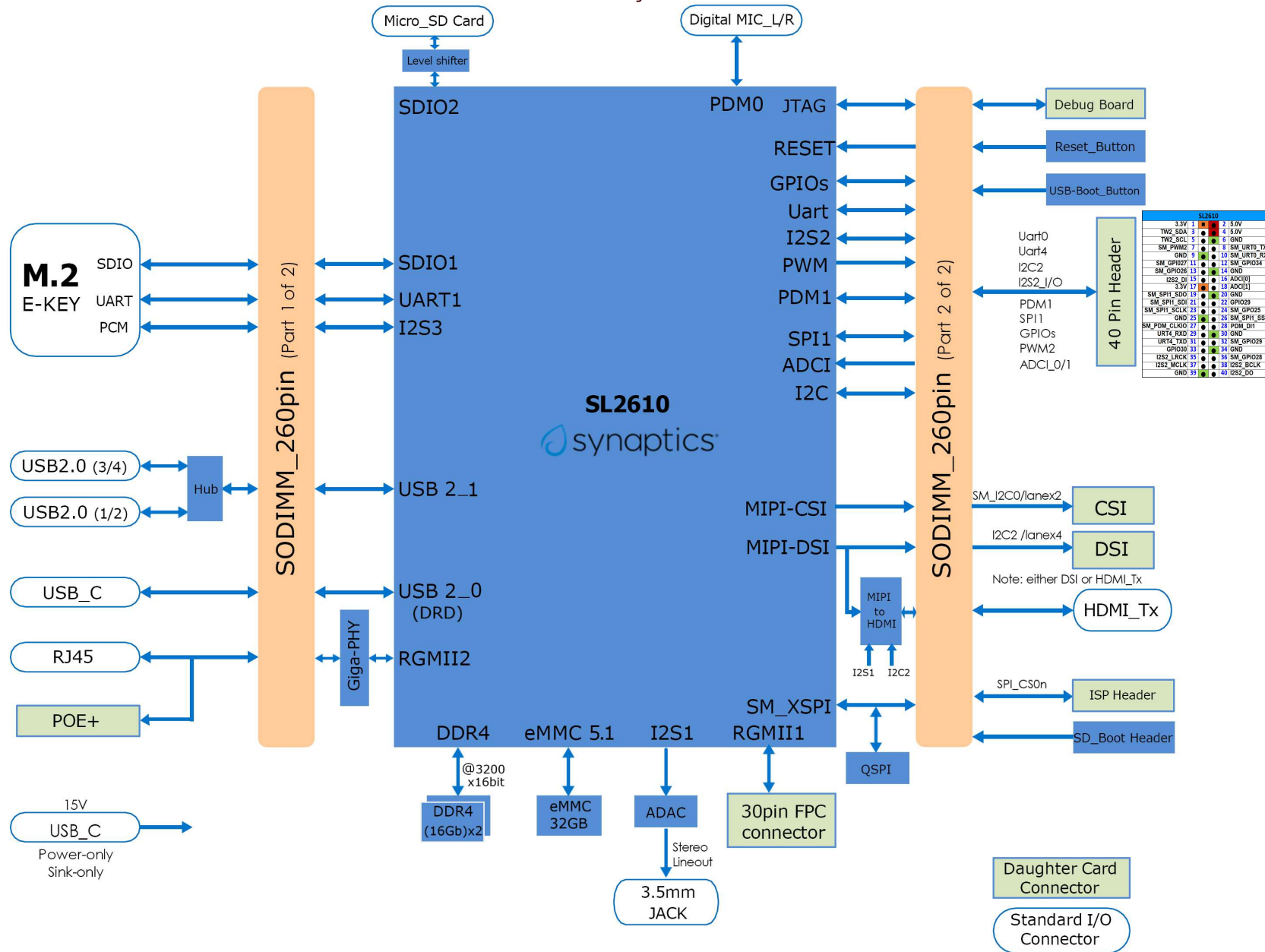


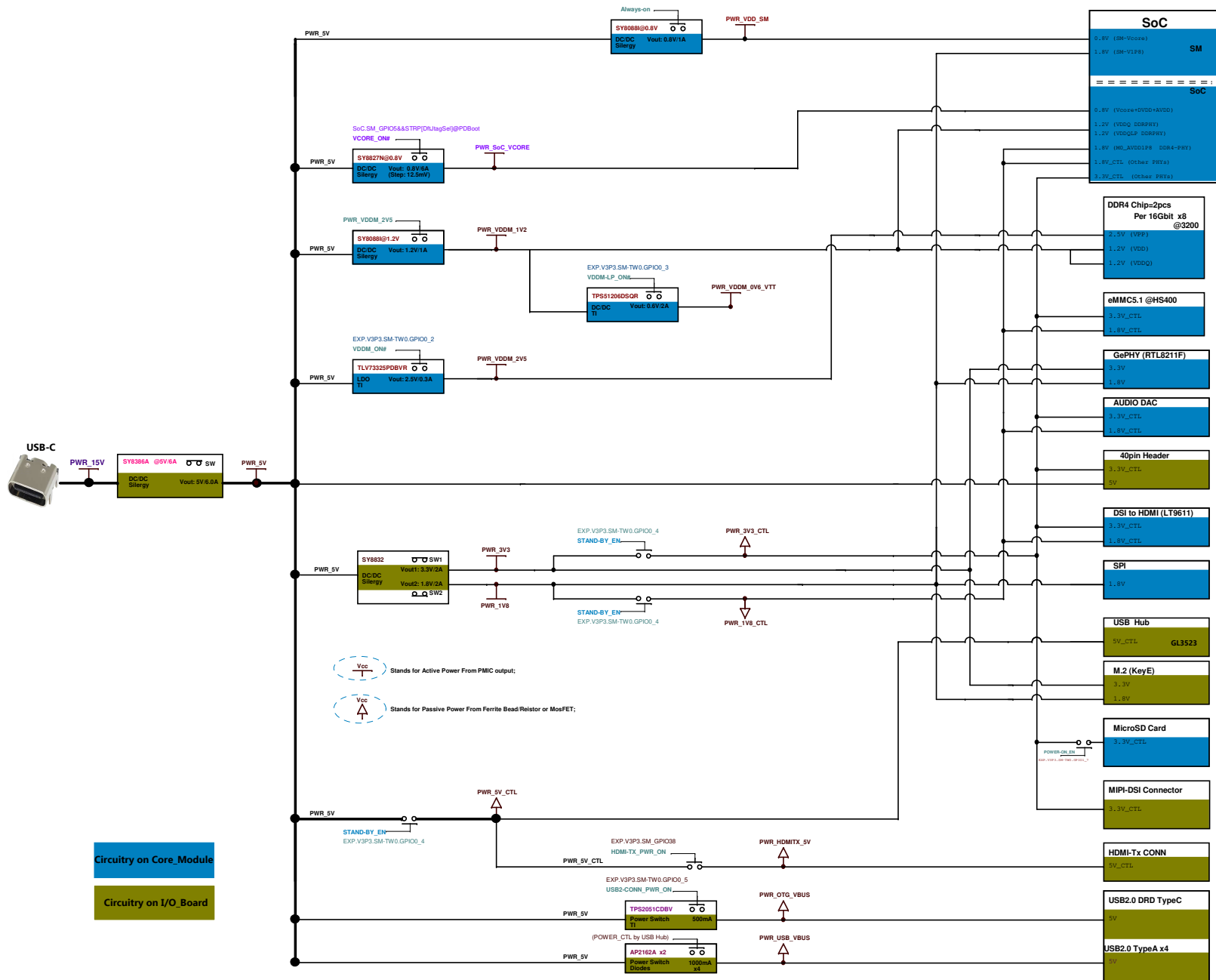
Table of Contents

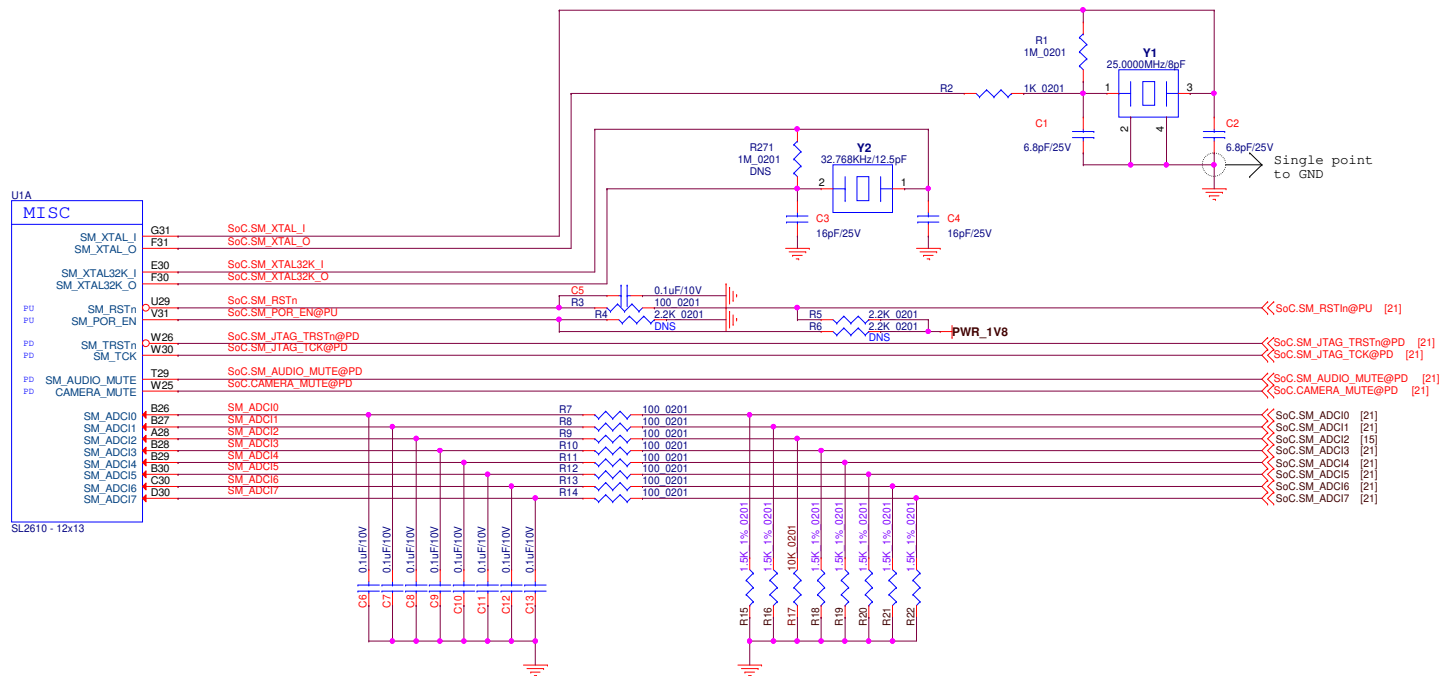
- 01: TITLE & BLOCK DIAGRM
- 02: REVISION HISTORY
- 03: POWER TREE
- 04: SL2610 - SM MISC
- 05: SL2610 - SOC MISC
- 06: SL1620 - DDR4_PHY
- 07: SL2610 - MIPI-CSI, MIPI-DSI
- 08: SL2610 - SDIO1, USB, eMMC
- 09: SL2610 - PWR/GND
- 10: SL2610 - STRAP
- 11: MEM - DEV DDR4
- 12: MEM - eMMC, SPI
- 13: PERIF - ETH_RTL8211F
- 14: PERIF - DSI_HDMI Converter
- 15: CONN - AUDIO DAC/DMIC
- 16: CONN - RGMII1
- 17: CONN - SD CARD
- 18: PWR - VDDM_2V5/1V2/VTT
- 19: PWR - VCORE/SM_VDD
- 20: Current-Measurement
- 21: SODIMM - GoldFinger

REVISION HISTORY

Rev#	Date	Originator(s)	Rev Item ID	What Revised	Why Revised	SW Impacts	Other Impacts	Rework# Base On Previous Version	SW Version SS[3:0]
A	04/10/2025	William W	1	SCH for SL2610 Core-Module	SL2610-RDK design	NO	NO		0001
B	10/11/2025	William W	1	Change R217 from 10K to 33K.	Optimize system power up sequence.	NO	NO	Rework-A	0000
			2	Add R274 2.2K pull-down resistor to STRP[plBypass]	Optimize design	NO	NO	Rework-B	
			3	Change L20 to 0R resistor.	Improve SDR50 performance	NO	NO	Rework-E	
			4	Change Pin-Demux for both SM_URT0 and SM_URT1 and rename net alias	Optimize design	Yes	NO		
			5	Update SOC symbol and add R276	Optimize design	NO	NO		
			6	Change R34 from DNS to 2.2K	SS[3:0] changes from 4'b0001 to 4'b0000	Yes	NO		

Power Tree





OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	BootStrap	SM_GPIO
SM_TMS	SM_GPIO0	SM_URTO_TXD	KEY_COL0	SM_PDM_DIO	SM_PWM10	SM_PWM10	SM_PWM10	...PUboot...	SM_GPIO0
SM_TDI	SM_GPIO1	SM_URTO_RXD	KEY_COL1	GPIO_TRIG0	SM_PWM9	KEY_ROW7	SM_PWM11	...PUboot...	SM_GPIO1
SM_TDO	SM_GPIO2	SM_PDM_CLKIO	T2S2_MCLK					...PUboot...	SM_GPIO2
SM_GPIO3	SM_SPI1_SS0n	SM_TW1_SCL	SM_PWM8	SM_I3C_MS_SCL					SM_GPIO3
SM_GPIO4	SM_SPI1_SS1n	SM_TW1_SDA	SM_PWM8	SM_I3C_MS_SDA					SM_GPIO4
SM_GPIO5	SM_SPI1_SS2n	SM_PWM1						dft_jtag_sel PUboot...	SM_GPIO5
SM_GPIO6	SM_SPI1_SS3n	SM_SPI15_SS0n	SM_PWM2						SM_GPIO6
SM_GPIO7	SM_URTO_RXD	SM_CAN0_RX	KEY_ROW6	GPIO_TRIG2	SM_PWM9	SM_UR1_RXD			SM_GPIO7
SM_GPIO8	SM_URTO_TXD	SM_CAN0_TX	SM_CLKOUT			SM_UR1_TXD		boot_src[0] PUboot...	SM_GPIO8
SM_GPIO9	SM_SPI1_SDO	SM_SPI15_SDO	SM_PWM3					boot_src[1] PUboot...	SM_GPIO9
SM_GPIO10	SM_SPI1_SCLK	SM_SPI15_SCLK	SM_PWM4						SM_GPIO10
SM_GPIO11	SM_SPI1_SDI	SM_SPI15_SDI	SM_PWM5						SM_GPIO11
SM_GPIO12	SM_TW0_SCL	SM_I3C_MS_SCL	SM_PWM6						SM_GPIO12
SM_GPIO13	SM_TW0_SDA	SM_I3C_MS_SDA	SM_CLKOUT						SM_GPIO13
SM_GPIO14	SM_TW1_SCL	SM_URTO_CTSn	SM_PWM10	SM_CAN0_RX		SM_UR1_CTSn			SM_GPIO14
SM_GPIO15	SM_TW1_SDA	SM_URTO_RTSn	SM_PWM11	SM_CAN0_TX		SM_UR1_RTSn			SM_GPIO15
SM_GPIO16	SM_TW1_RXD	SM_CAN0_RX	SM_PWM7						SM_GPIO16
SM_GPIO17	SM_UR1_TXD	SM_CAN0_TX	SM_PWM8			SM_UR0_TXD		pll_bypass PUboot...	SM_GPIO17
SM_GPIO18	SM_XSPI_CS0n								SM_GPIO18
SM_GPIO19	SM_XSPI_DATA0								SM_GPIO19
SM_GPIO20	SM_XSPI_DATA1								SM_GPIO20
SM_GPIO21	SM_XSPI_DATA2								SM_GPIO21
SM_GPIO22	SM_XSPI_DATA3								SM_GPIO22
SM_GPIO23	SM_XSPI_CLK								SM_GPIO23
SM_GPIO24	SM_XSPI_CLKn								SM_GPIO24
SM_GPIO25	SM_XSPI_CS0n	SM_UR2_TXD	KEY_COL2	SM_UR3_RTSn	SM_UR3_DE	KEY_ROW6	SM_CLKOUT		SM_GPIO25
SM_GPIO26	SM_XSPI_DATA4	SM_UR2_RXD	KEY_COL3	SM_UR3_CTSn	SM_UR3_REn	KEY_ROW4			SM_GPIO26
SM_GPIO27	SM_XSPI_DATA5	SM_UR3_TXD	KEY_COL4	SM_UR2_RTSn	SM_UR0_RTSn	KEY_ROW3	SM_UR1_RTSn		SM_GPIO27
SM_GPIO28	SM_XSPI_DATA6	SM_UR3_RXD	KEY_COL5	SM_UR2_CTSn	SM_UR0_CTSn	KEY_ROW2	SM_UR1_CTSn		SM_GPIO28
SM_GPIO29	SM_XSPI_DATA7		KEY_COL6				SM_CLKOUT		SM_GPIO29
SM_GPIO30	SM_XSPI_CS0n								SM_GPIO30
SM_GPIO31	SM_XSPI_CS1n								SM_GPIO31
SM_GPIO32	SM_XSPI_CS2n								SM_GPIO32
SM_GPIO33	SM_XSPI_CS3n								SM_GPIO33
SM_GPIO34	SM_XSPI_CS4n								SM_GPIO34
SM_GPIO35	SM_XSPI_CS5n								SM_GPIO35
SM_GPIO36	SM_XSPI_CS6n								SM_GPIO36
SM_GPIO37	SM_XSPI_CS7n								SM_GPIO37
SM_GPIO38	SM_XSPI_CS8n								SM_GPIO38

U1E		OPT1	OPT2	OPT3	OPT4	OPT5	OPT6	OPT7	OPT8	BootStrap	GPIO
GPI00		I2S1_LRCK							SPI3_SS0n		GPI00
GPI01		I2S1_BCLK							SPI3_SCLK		GPI01
GPI02		I2S1_DO							SPI3_SDO		GPI02
GPI03		I2S1_MCLK							SPI3_SS1n		GPI03
GPI04		I2S1_DI							SPI3_SDI		GPI04
GPI05		I2S2_LRCK	CAM_FIXCLK	KEY_ROW0	SPDIFI			KEY_ROW7			GPI05
GPI06		I2S2_BCLK	CAM_HSYNC	KEY_ROW1	SPDIFO			KEY_ROW5			GPI06
GPI07		I2S2_DO		KEY_ROW2	SPDIFO		SM_PDM_CLKIO	KEY_ROW5			GPI07
GPI08		I2S2_DI	CAM_VSYNC	KEY_ROW3	SPDIFI			KEY_COL4			GPI08
GPI09			CAM_DATA0		PDM_DI1						GPI09
GPI010			CAM_DATA1		PDM_DI2		DSI_TE				GPI010
GPI011		I2S2_MCLK	CMA_DATA2		SM_PDM_CLKIO						GPI011
GPI012		I2S3_LRCK	CAM_DATA3		SDIO2_WP						GPI012
GPI013		I2S3_BCLK	PDM_DI1		RGMII_PTP_PFS_USB2_DRV_VBUS						GPI013
GPI014		I2S3_DO			PDM_DI3				SPDIFO		GPI014
GPI015		I2S3_DI	CAM_DATA4		SM_PDM_DI0				SPDIFI		GPI015
GPI016		SPI2_SS0n			SDIO2_DAT3						GPI016
GPI017		SPI2_SS1n	CAM_DATA5		SDIO2_DAT2		DSI_TE				GPI017
GPI018		SPI2_SS2n	CAM_DATA6		SDIO2_DAT1	PDM_DI2	SM_CAN1_RX				GPI018
GPI019		SPI2_SS3n	CAM_DATA7		SDIO2_DAT0	PDM_DI3	SM_CAN1_TX				GPI019
GPI020		SPI2_SDO			SDIO2_CMD						GPI020
GPI021		SPI2_SCLK			SDIO2_CLK		CLKOUT			software_strap[1]_PDBoot	GPI021
GPI022		SPI2_SDI			SDIO2_Cdn	SDIO1_Cdn					GPI022
GPI023		TW2_SCL	RGMII_MDC		KEY_ROW0		SPI3_SS2n	KEY_COL3			GPI023
GPI024		TW2_SDA	RGMII_MDIO		KEY_ROW1		SPI3_SS3n	KEY_COL2			GPI024
GPI025		URT5_RXD	GPI0_TRIG1		KEY_ROW2		SM_URT1_RXD	KEY_COL1			GPI025
GPI026		URT5_TXD	RGMII_PTP_PFS_0				USB2_DRV_VBUS			cpu_fat_bypass_PDBoot	GPI026
GPI027		TW3_SCL	URT4_TXD				SM_URT1_TXDn				GPI027
GPI028		TW3_SDA	URT4_RXD				SM_URT1_CTSn				GPI028
GPI029			URT4_DE		KEY_ROW4			KEY_COL4	SPI4_SDI		GPI029
GPI030			URT4_REn		KEY_ROW5			KEY_COL5	SPI4_SCLK		GPI030
GPI031			RGMII_MDC				SPI5_SS3n	SPI3_SS2n	SPI4_SS2n		GPI031
GPI032			RGMII_MDIO					SPI3_SS3n	SPI4_SS3n		GPI032
GPI033		RGMII1_TD0	RMI11_TXD0				SM_CAN0_TX	SPI3_SS1n	SPI4_SS1n	software_strap[2]_PDBoot	GPI033
GPI034		RGMII1_TD1	RMI11_TXD1				SM_CAN0_RX				GPI034
GPI035		RGMII1_TD2	RMI12_TXD0	KEY_COL7	URT5_RXD				SPI4_SS0n		GPI035
GPI036		RGMII1_TD3	RMI12_TXD1		URT5_TXD				SPI4_SDO	software_strap[3]_PDBoot	GPI036
GPI037		RGMII1_RD0	RMI11_RXD0				SM_CAN1_TX		SPI5_SDI		GPI037
GPI038		RGMII1_RD1	RMI11_RXD1				SM_CAN1_RX		SPI5_SDO		GPI038
GPI039		RGMII1_RD2	RMI12_RXD0	KEY_ROW6	URT6_RXD	SPI5_SS1n		SPI4_SS3n			GPI039
GPI040		RGMII1_RD3	RMI12_RXD1	KEY_ROW7	URT6_TXD	SPI5_SS2n		SPI4_SS2n			GPI040
GPI041		RGMII1_RXC	RMI11_CRSDV						SPI5_SCLK		GPI041
GPI042		RGMII1_TXC	RMI12_CRSDV	KEY_ROW8	URT7_RXD			SPI4_SCLK			GPI042
GPI043		RGMII1_TXCTL	RMI11_TXEN					SPI4_SS0n		software_strap[0]_PUBoot	GPI043
GPI044		RGMII1_RXCTL	RMI12_TXEN	KEY_ROW9	URT7_TXD			SPI4_SDI			GPI044
GPI045		RGMII1_CLKOUT	RMI11_REFCLK								GPI045
GPI046		SDIO1_Cdn	SDIO2_Cdn	KEY_COL0		SM_URT1_RSTn	KEY_ROW9	DSI_TE			GPI046
GPI047		SDIO1_WP	SDIO2_WP	KEY_COL1	RMI12_REFCLK	SM_URT1_CTS	KEY_ROW8				GPI047
GPI048		RGMII2_TD0				SPI5_SS0n	SPI4_SS2n	SPI3_SS3n			GPI048
GPI049		RGMII2_TD1				SPI5_SDO	SPI4_SS3n	SPI3_SS2n			GPI049
GPI050		RGMII2_TD2				SPI5_SCLK		SPI3_SS1n			GPI050
GPI051		RGMII2_TD3						SPI3_SS0n			GPI051
GPI052		RGMII2_RD0						SPI4_SS2n	SPI3_SDO		GPI052
GPI053		RGMII2_RD1						SPI4_SS3n	SPI3_SCLK		GPI053
GPI054		RGMII2_RD2						SPI3_SDI			GPI054
GPI055		RGMII2_RD3				SPI5_SDI		SPI4_SS1n			GPI055
GPI056		RGMII2_RXC						SPI4_SS0n			GPI056
GPI057		RGMII2_TXC						SPI4_SDO			GPI057
GPI058		RGMII2_TXCTL						SPI4_SCLK			GPI058
GPI059		RGMII2_RXCTL						SPI4_SDI			GPI059


SL2610 - 12x13

AA31	SoC.I2S1_LRCK	>>SoC.I2S1_LRCK [14,15]
AA29	SoC.I2S1_BCLK	>>SoC.I2S1_BCLK [14,15]
AA30	SoC.I2S1_DO	>>SoC.I2S1_DO [14,15]
W29	SoC.I2S1_MCLK	>>SoC.I2S1_MCLK [14]
AB30	SoC.GPI04	>>SoC.GPI04 [21]
AC31	SoC.I2S2_LRCK	>>SoC.I2S2_LRCK [21]
AC30	SoC.I2S2_BCLK	>>SoC.I2S2_BCLK [21]
AA26	SoC.I2S2_DO	>>SoC.I2S2_DO [21]
AA25	SoC.I2S2_DI	>>SoC.I2S2_DI [21]
AB28	SoC.PDM_DI1	>>SoC.PDM_DI1 [21]
AE30	SoC.GPI010	>>SoC.GPI010 [14]
AD30	SoC.GPI011.SM_PDM_CLKIO	>>SoC.GPI011.SM_PDM_CLKIO [21]
AE24	SoC.I2S3_LRCK	>>SoC.I2S3_LRCK [21]
AC27	SoC.I2S3_BCLK	>>SoC.I2S3_BCLK [21]
AF30	SoC.I2S3_DO	>>SoC.I2S3_DO [21]
AC25	SoC.I2S3_DI	>>SoC.I2S3_DI [21]
AG30	SoC.SPI2_SS0n&SDIO2_DAT3	>>SoC.SPI2_SS0n&SDIO2_DAT3 [17]
AG28	SoC.SPI2_SS1n&SDIO2_DAT2	>>SoC.SPI2_SS1n&SDIO2_DAT2 [17]
AG29	SoC.SPI2_SS2n&SDIO2_DAT1	>>SoC.SPI2_SS2n&SDIO2_DAT1 [17]
AF31	SoC.SPI2_SS3n&SDIO2_DAT0	>>SoC.SPI2_SS3n&SDIO2_DAT0 [17]
AH28	SoC.SPI2_SDO&SDIO2_CMD	>>SoC.SPI2_SDO&SDIO2_CMD [17]
AF27	SoC.SPI2_SCLK&SDIO2_CLK&&STRP[SS1]@PDBoot	>>SoC.SPI2_SCLK&SDIO2_CLK&&STRP[SS1]@PDBoot [10,17]
AF28	SoC.SPI2_SDI&SDIO2_Cdn	>>SoC.SPI2_SDI&SDIO2_Cdn [17]
B4	SoC.TW2_SCL	>>SoC.TW2_SCL [14,21]
B3	SoC.TW2_SDA	>>SoC.TW2_SDA [14,21]
C6	SoC.GPI025	>>SoC.GPI025 [14]
C5	SoC.GPI026&&STRP[cpuRstByps]@PDBoot	>>SoC.GPI026&&STRP[cpuRstByps]@PDBoot [10,15]
A3	SoC.URT4_TXD	>>SoC.URT4_TXD [21]
B2	SoC.URT4_RXD	>>SoC.URT4_RXD [21]
A6	SoC.GPI029	>>SoC.GPI029 [21]
B6	SoC.GPI030	>>SoC.GPI030 [21]
C7	SoC.RGMII_MDC	>>SoC.RGMII_MDC [13,16]
B7	SoC.RGMII_MDIO	>>SoC.RGMII_MDIO [13,16]
C8	SoC.RGMII1_TD0&&STRP[SS2]@PDBoot	>>SoC.RGMII1_TD0&&STRP[SS2]@PDBoot [10,16]
F10	SoC.RGMII1_TD1	>>SoC.RGMII1_TD1 [16]
C9	SoC.RGMII1_TD2	>>SoC.RGMII1_TD2 [16]
B9	SoC.RGMII1_TD3&&STRP[SS3]@PDBoot	>>SoC.RGMII1_TD3&&STRP[SS3]@PDBoot [10,16]
B10	SoC.RGMII1_RD0	>>SoC.RGMII1_RD0 [16]
F13	SoC.RGMII1_RD1	>>SoC.RGMII1_RD1 [16]
D11	SoC.RGMII1_RD2	>>SoC.RGMII1_RD2 [16]
A9	SoC.RGMII1_RD3	>>SoC.RGMII1_RD3 [16]
B11	SoC.RGMII1_RXC	>>SoC.RGMII1_RXC [16]
B12	SoC.RGMII1_TXC	>>SoC.RGMII1_TXC [16]
B13	SoC.RGMII1_TXCTL&&STRP[SS0]@PUBoot	>>SoC.RGMII1_TXCTL&&STRP[SS0]@PUBoot [10,16]
C13	SoC.RGMII1_RXCTL	>>SoC.RGMII1_RXCTL [16]
A13	SoC.RGMII1_CLKOUT	>>SoC.RGMII1_CLKOUT [16]
C14	SoC.GPI046	>>SoC.GPI046 [21]
B14	SoC.RMI12_REFCLK	>>SoC.RMI12_REFCLK [16]
F15	SoC.RGMII2_TXD0	>>SoC.RGMII2_TXD0 [13]
F17	SoC.RGMII2_TXD1	>>SoC.RGMII2_TXD1 [13]
C15	SoC.RGMII2_TXD2	>>SoC.RGMII2_TXD2 [13]
D15	SoC.RGMII2_TXD3	>>SoC.RGMII2_TXD3 [13]
B16	SoC.RGMII2_RXD0	>>SoC.RGMII2_RXD0 [13]
A16	SoC.RGMII2_RXD1	>>SoC.RGMII2_RXD1 [13]
C17	SoC.RGMII2_RXD2	>>SoC.RGMII2_RXD2 [13]
C19	SoC.RGMII2_RXD3	>>SoC.RGMII2_RXD3 [13]
B17	SoC.RGMII2_RXC	>>SoC.RGMII2_RXC [13]
A18	SoC.RGMII2_TXC	>>SoC.RGMII2_TXC [13]
B19	SoC.RGMII2_TXCTL	>>SoC.RGMII2_TXCTL [13]
B18	SoC.RGMII2_RXCTL	>>SoC.RGMII2_RXCTL [13]

LT9611-IN7n

Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131



Title

SL2610 CORE MODULE

Size

Document Number

Rev

CS950-C01132-01

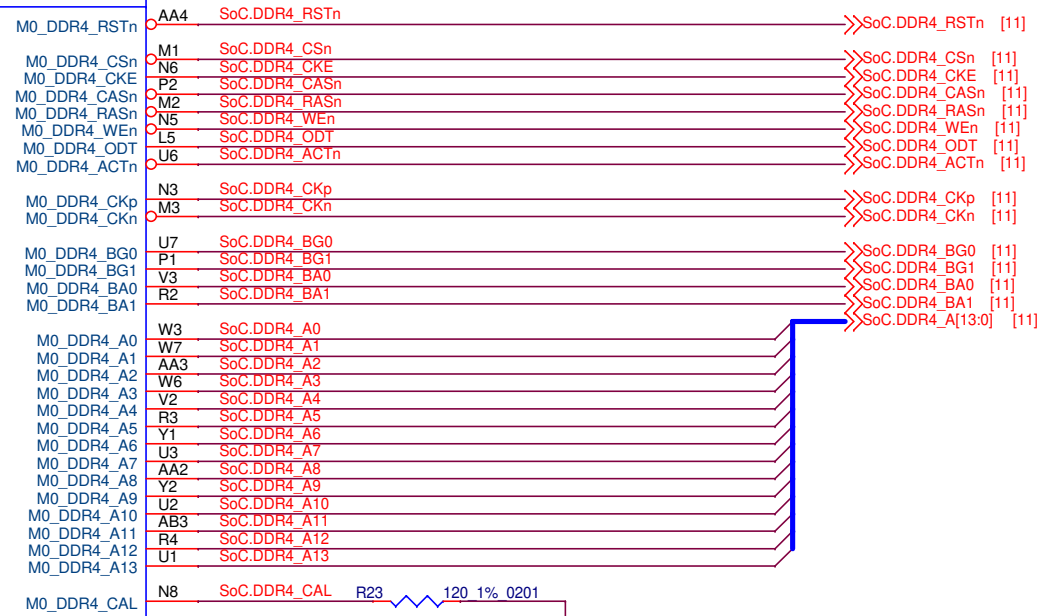
B

Date: Thursday, October 23, 2025

Sheet 5 of 21

U1B

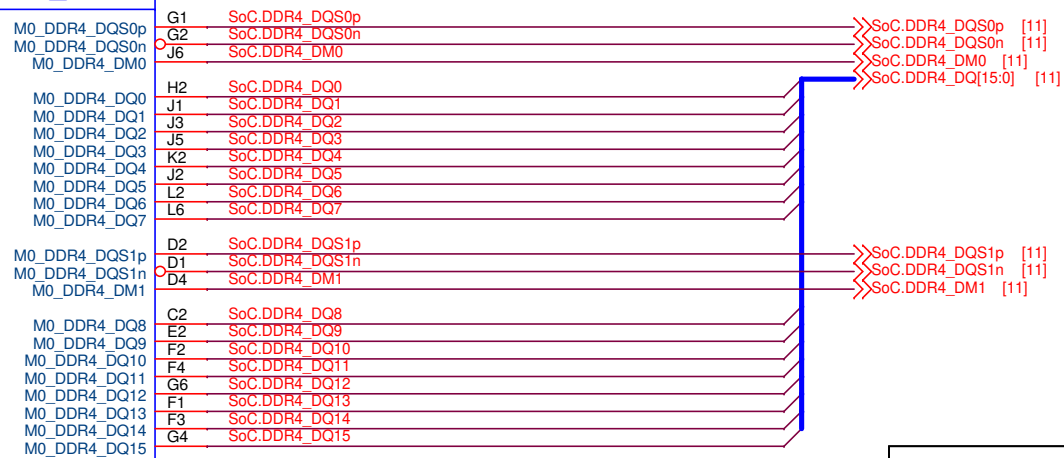
DDR4_SDRAM



SL2610 - 12x13

U1C

DDR4_SDRAM



SL2610 - 12x13

Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131



Title

SL2610 CORE MODULE

Size

Document Number

SC950-C01132-01

Rev

B

Date:

Thursday, October 23, 2025

Sheet

6

of

21

U1G

MIPI - CSI

MIPI_CSI_CKp
MIPI_CSI_CKnMIPI_CSI_D0p
MIPI_CSI_D0n
MIPI_CSI_D1p
MIPI_CSI_D1n

MIPI_CSI_REXT

AH19 SoC.MIPI_CSI_CKp

AG19 SoC.MIPI_CSI_CKn

AH17 SoC.MIPI_CSI_D0p

AG17 SoC.MIPI_CSI_D0n

AG15 SoC.MIPI_CSI_D1p

AG16 SoC.MIPI_CSI_D1n

AC17 R24 200 1% 0201

<< SoC.MIPI_CSI_CKp [21]

<< SoC.MIPI_CSI_CKn [21]

<< SoC.MIPI_CSI_D0p [21]

<< SoC.MIPI_CSI_D0n [21]

<< SoC.MIPI_CSI_D1p [21]

<< SoC.MIPI_CSI_D1n [21]

SL2610 - 12x13

U1H

MIPI - DSI

MIPI_DSI_CKp
MIPI_DSI_CKnMIPI_DSI_D0p
MIPI_DSI_D0n
MIPI_DSI_D1p
MIPI_DSI_D1n
MIPI_DSI_D2p
MIPI_DSI_D2n
MIPI_DSI_D3p
MIPI_DSI_D3n

MIPI_DSI_REXT

AF23 SoC.MIPI_DSI_TCKp

AF24 SoC.MIPI_DSI_TCKn

AG26 SoC.MIPI_DSI_TD0p

AH26 SoC.MIPI_DSI_TD0n

AH24 SoC.MIPI_DSI_TD1p

AG24 SoC.MIPI_DSI_TD1n

AG22 SoC.MIPI_DSI_TD2p

AH22 SoC.MIPI_DSI_TD2n

AG20 SoC.MIPI_DSI_TD3p

AG21 SoC.MIPI_DSI_TD3n

AA19 R25 200 1% 0201

>> SoC.MIPI_DSI_TCKp [14]

>> SoC.MIPI_DSI_TCKn [14]

>> SoC.MIPI_DSI_TD0p [14]

>> SoC.MIPI_DSI_TD0n [14]

>> SoC.MIPI_DSI_TD1p [14]

>> SoC.MIPI_DSI_TD1n [14]

>> SoC.MIPI_DSI_TD2p [14]

>> SoC.MIPI_DSI_TD2n [14]

>> SoC.MIPI_DSI_TD3p [14]

>> SoC.MIPI_DSI_TD3n [14]

SL2610 - 12x13

Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131

Title

SL2610 CORE MODULE

Size

Document Number

SC950-C01132-01

Rev

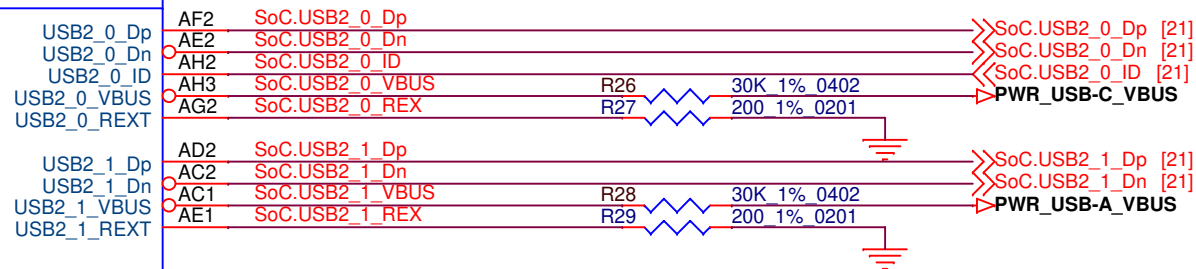
B

Date: Thursday, October 23, 2025

Sheet 7 of 21

U1F

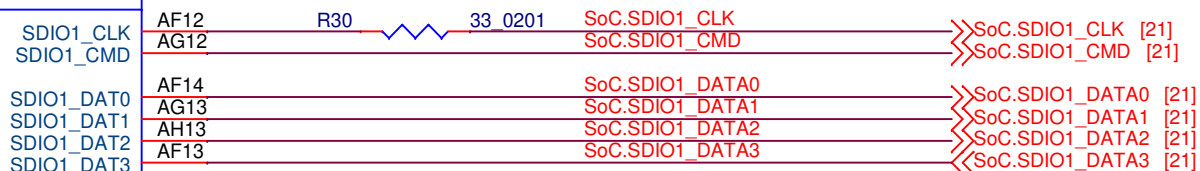
USB2



SL2610 - 12x13

U1J

SDIO1



SL2610 - 12x13

To M.2

U1I

EMMC



SL2610 - 12x13

Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131

Title

SL2610 CORE MODULE

Size

Document Number

SC950-C01132-01

Rev

B

Date:

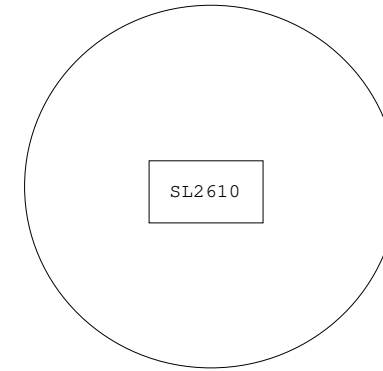
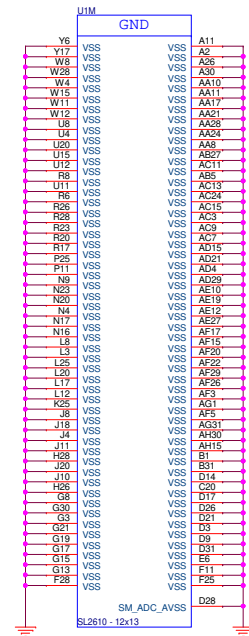
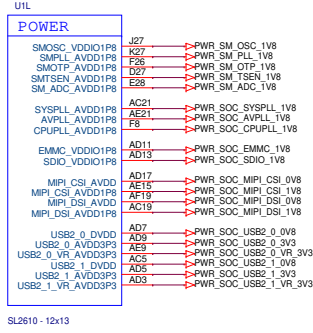
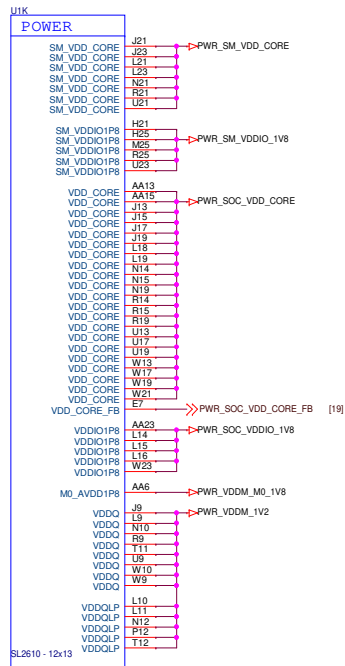
Thursday, October 23, 2025

Sheet

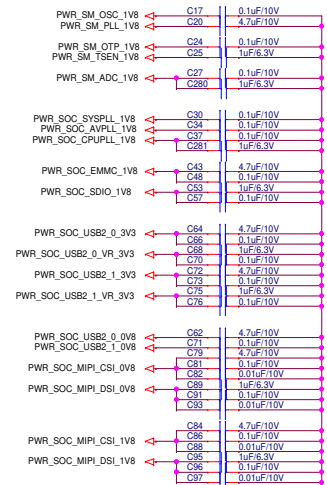
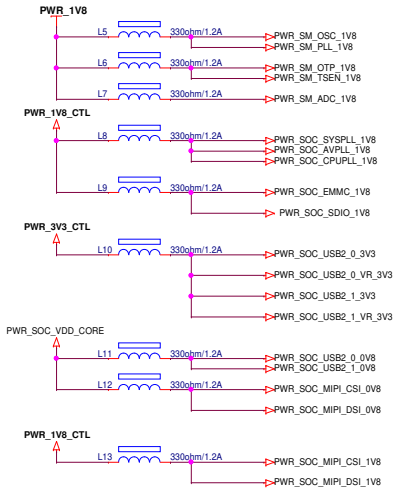
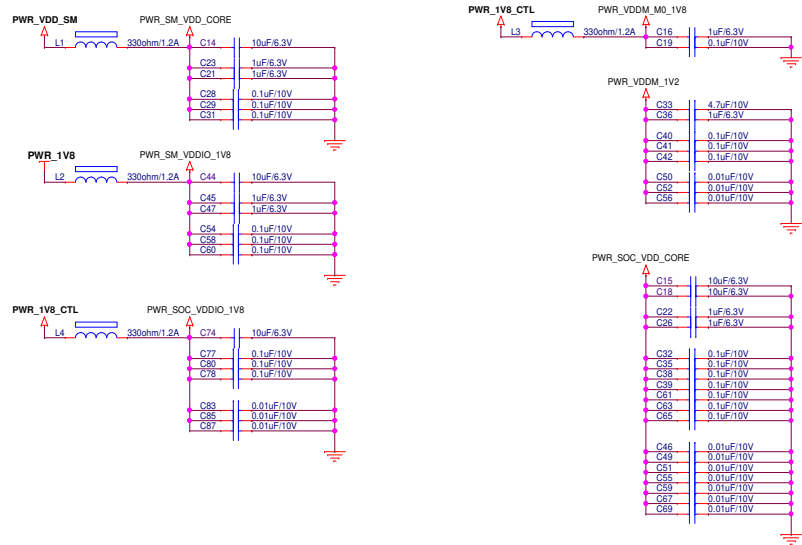
8

of

21



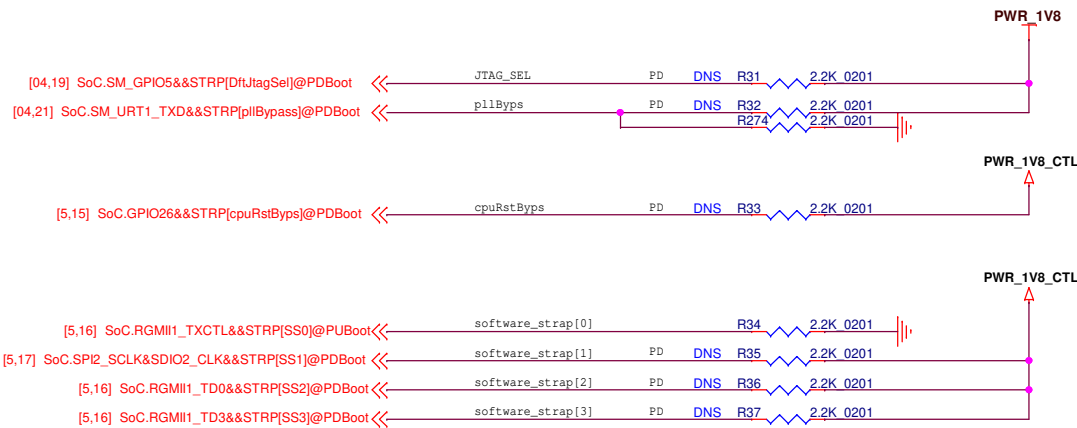
The components inside 80mm diameter area can not be higher than 17.7mm



Synaptics, Inc.
 1109 McKay Dr.
 SAN JOSE, CA 95131



Title SL2610 CORE MODULE		
Size	Document Number SC950-C01132-01	Rev B
Date:	Thursday, October 23, 2025	Sheet 9 of 21



JTAG_SEL 0: ATE/RMA Mode - but Functional JTAG is selected
1: ATE/RMA Mode - DFT JTAG is selected

pllByps 0: No Bypass (Default)
1: All PLL bypassed

cpuRstByps 0: Enable reset logic inside cpu partition (Default)
1: Bypass reset logic inside cpu partition

software_strap[0]
Default: 0

software_strap[1]
Default: 0

software_strap[2]
Default: 0

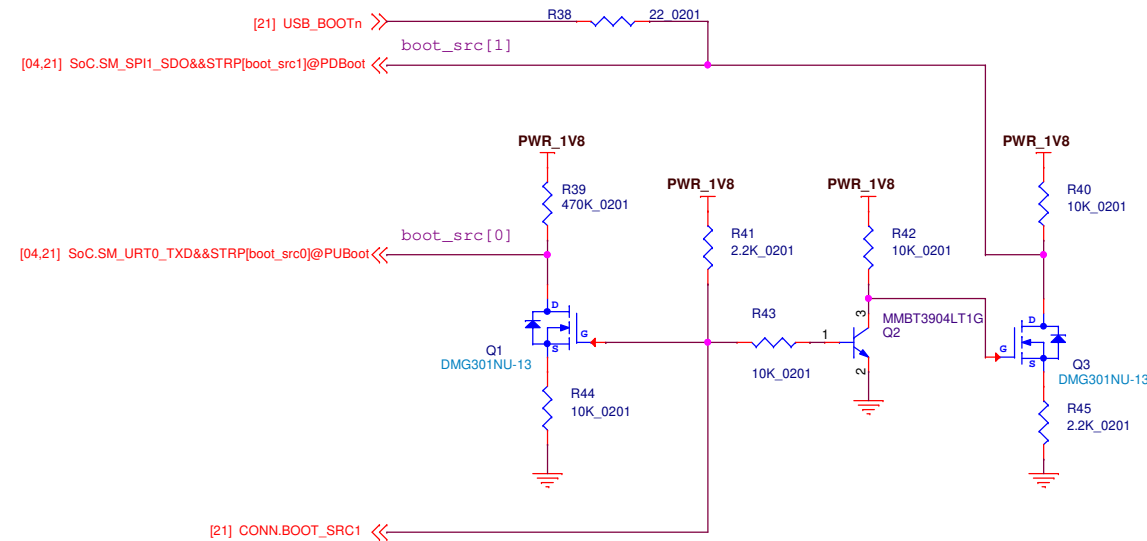
software_strap[3]
Default: 0

BOOT STRAP OPTION

BootSrc[1:0]	TYPE
2'b00	ROM boot from USB2
2'b01	ROM boot from xSPI_NOR
2'b10	ROM boot from EMMC default
2'b11	ROM boot from xSPI_NAND

Note for xSPI_NAND
1. CONN-VDDIO1P8.BOOT_SRC1 = Low (external SPI board header JP10 2-3 is ON)
2. HW rework Q3.G to GND

Note for SPI Clear_Boot
1. CONN-VDDIO1P8.BOOT_SRC1 = Low (external SPI board header JP10 2-3 is ON)
2. HW rework Q3.G to GND
3. HW rework R33=2.2K (cpuRstByp = 1)

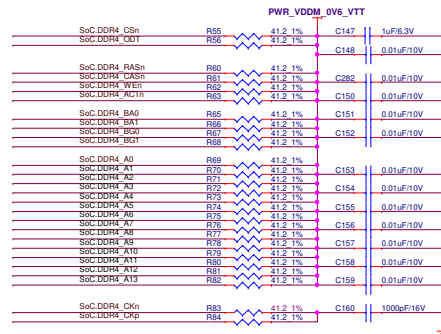
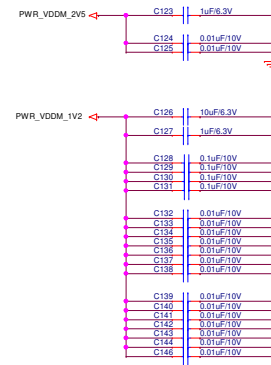
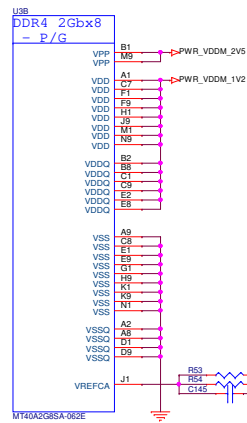
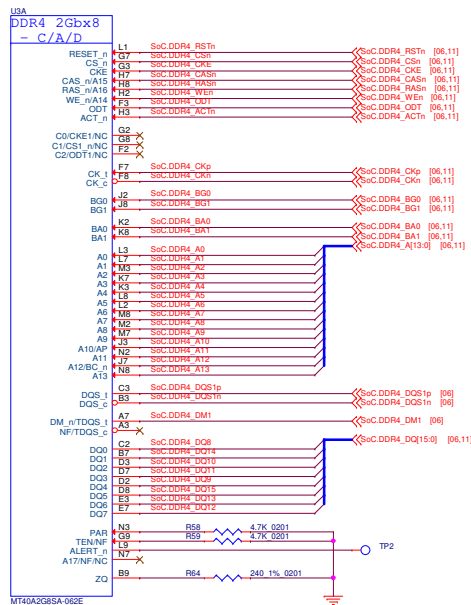
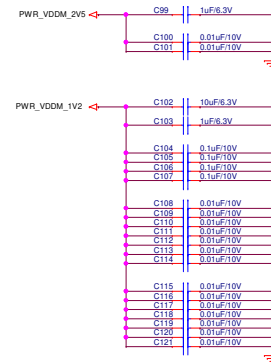
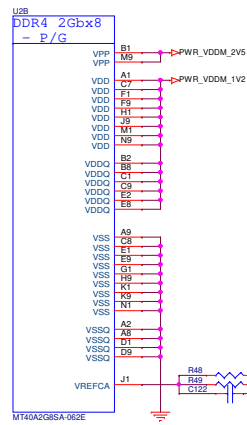
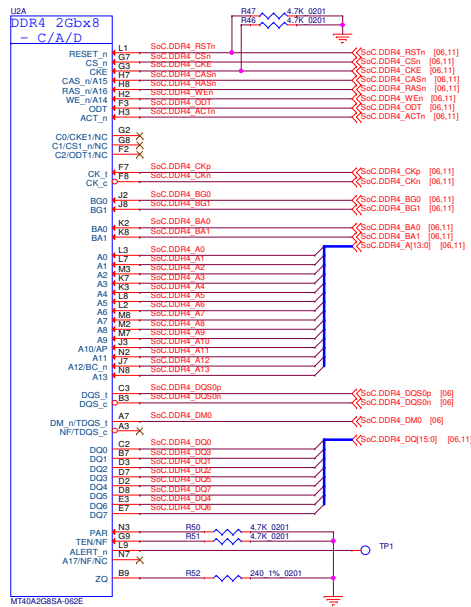


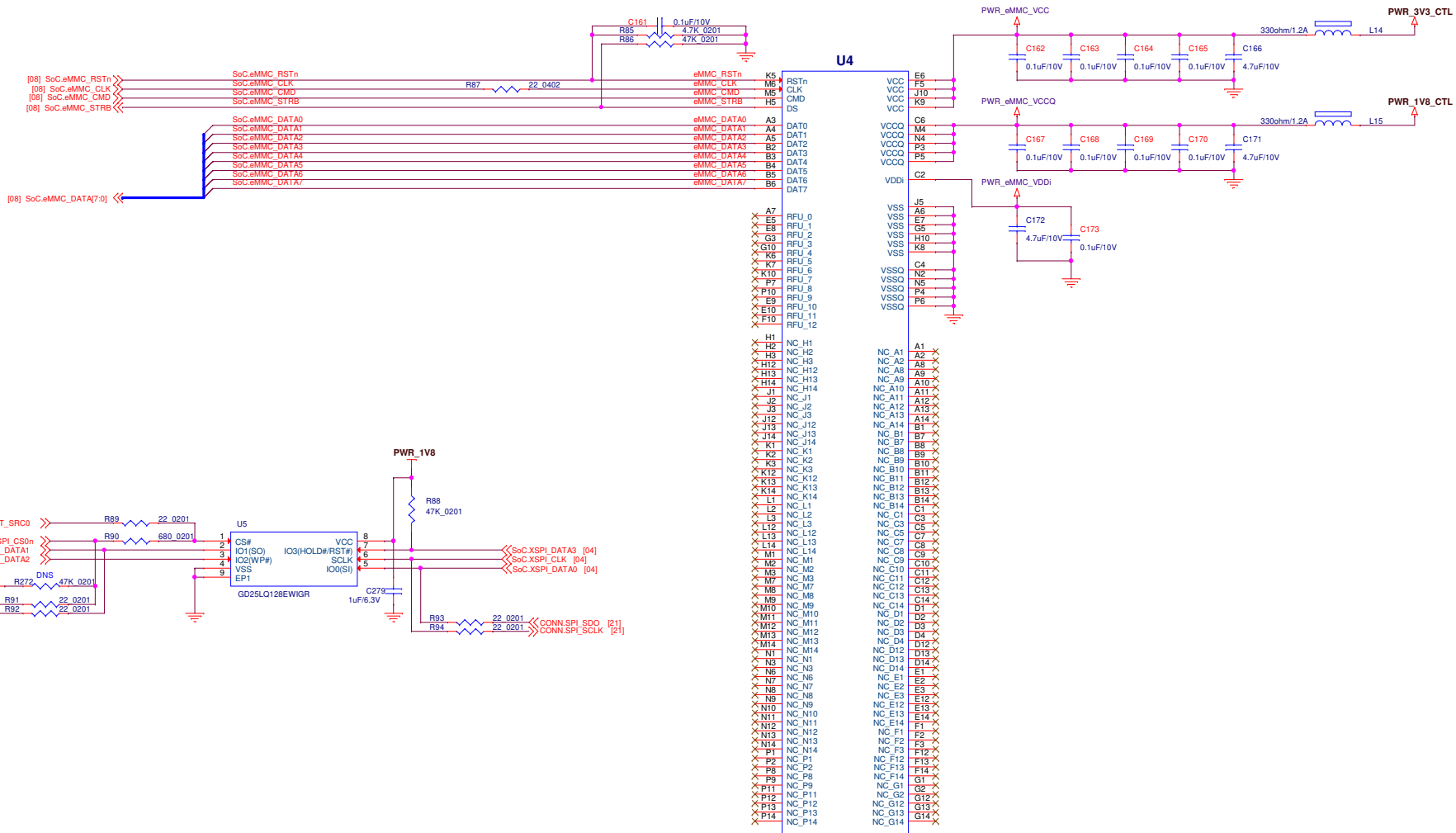
Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131



Title SL2610 CORE MODULE		
Size	Document Number SC950-C01132-01	Rev B
Date:	Thursday, October 23, 2025	Sheet 10 of 21





MTF32GBCAQTC-IT

Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131

synaptics

Title

SL2610 CORE MODULE

Size

Document Number

SC950-C01132-01

Rev

B

Date:

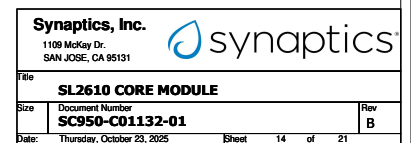
Thursday, October 23, 2025

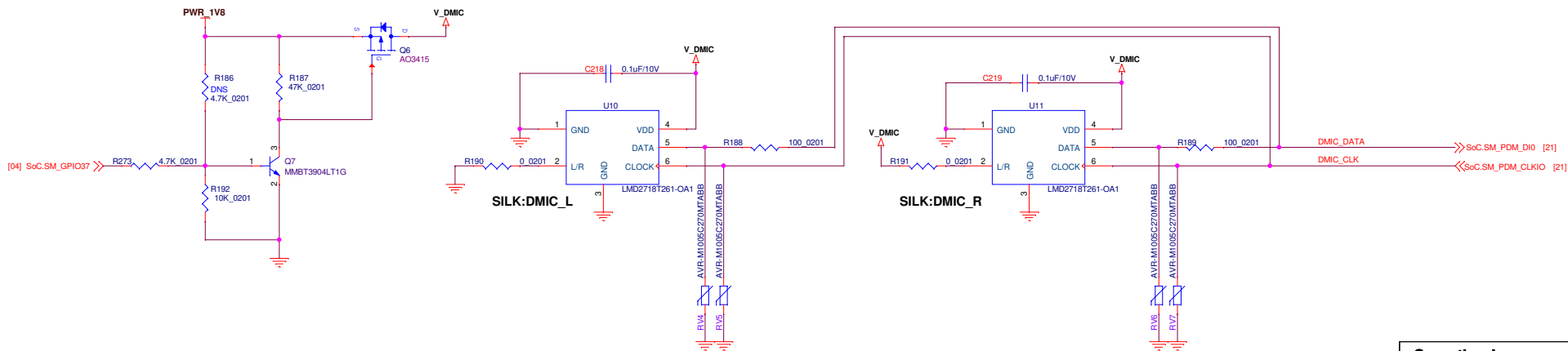
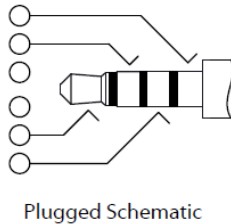
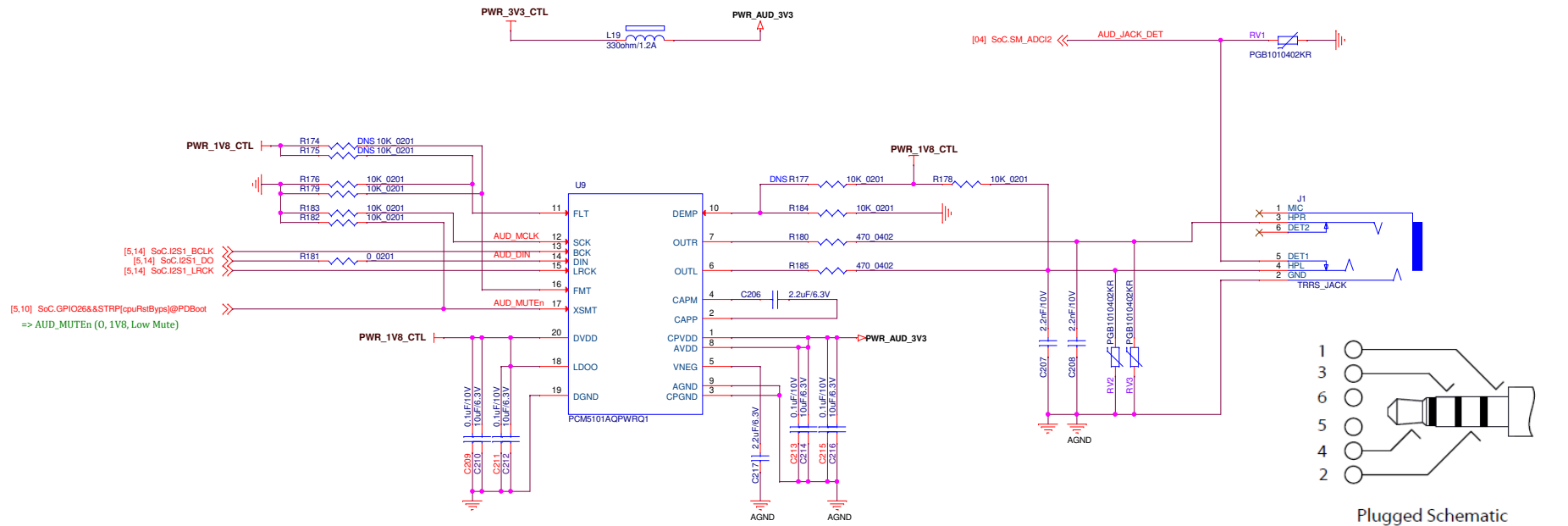
Sheet

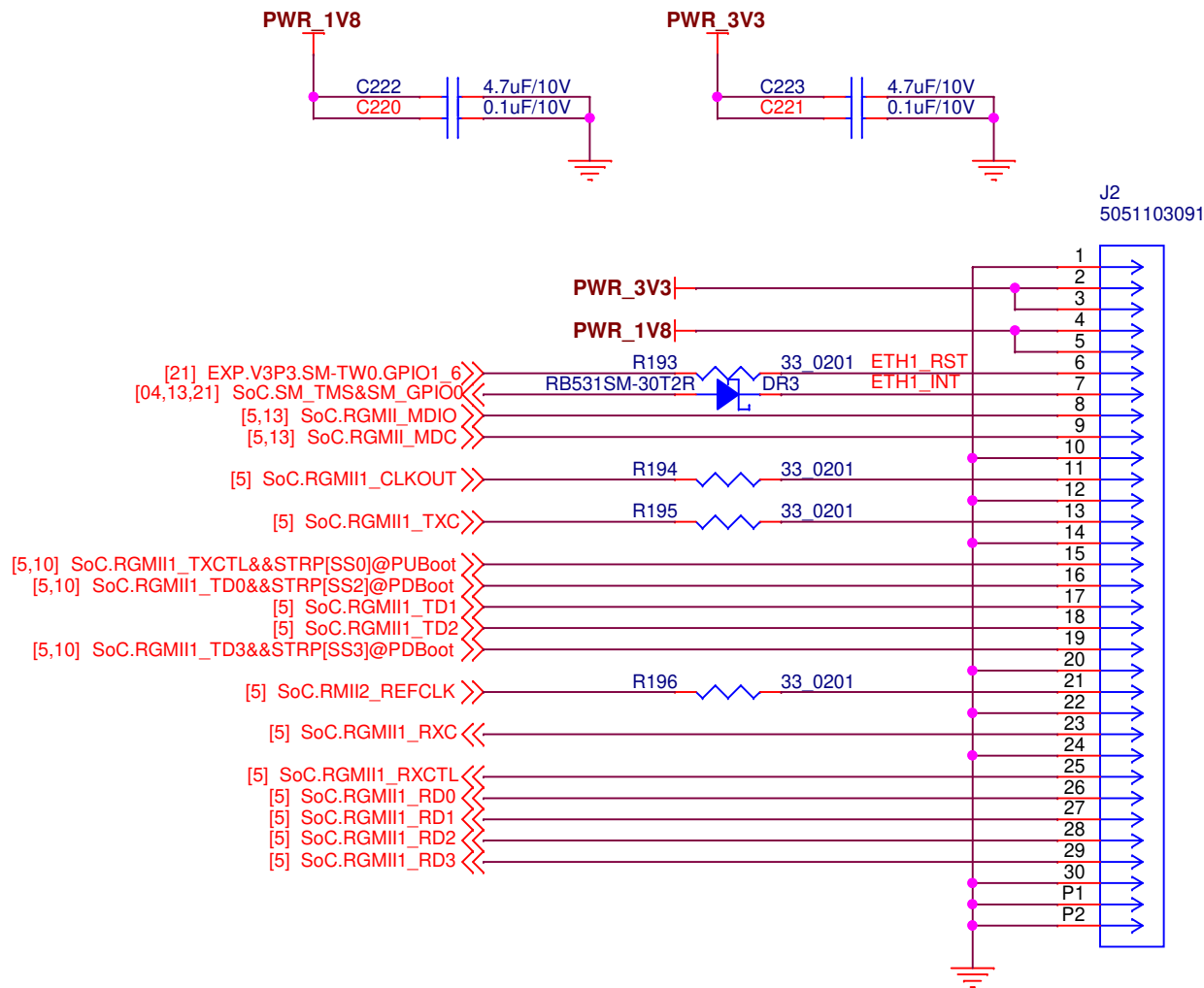
12

of

21







Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131



Title

SL2610 CORE MODULE

Size

Document Number

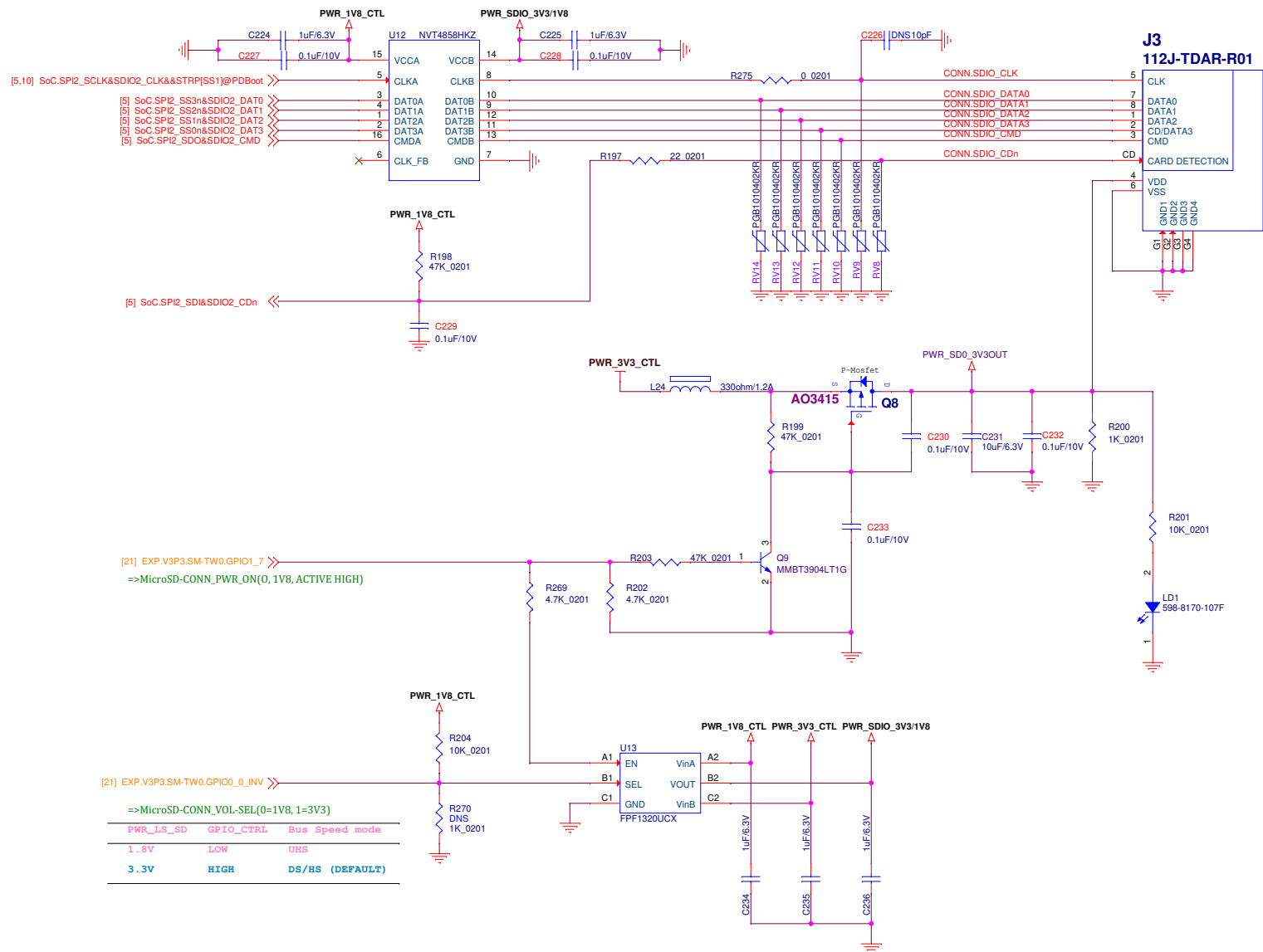
SC950-C01132-01

Rev

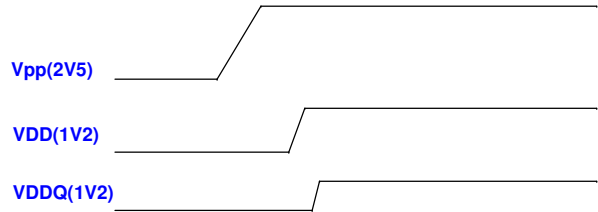
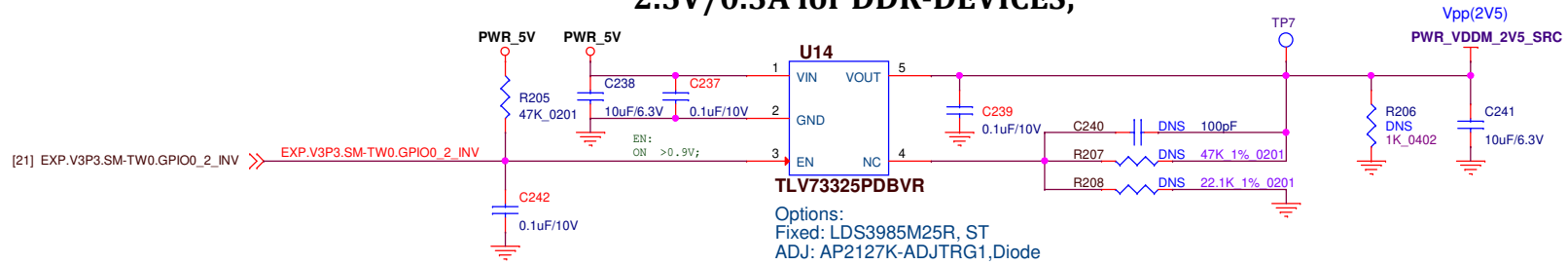
B

Date: Thursday, October 23, 2025

Sheet 16 of 21



2.5V/0.3A for DDR-DEVICES;

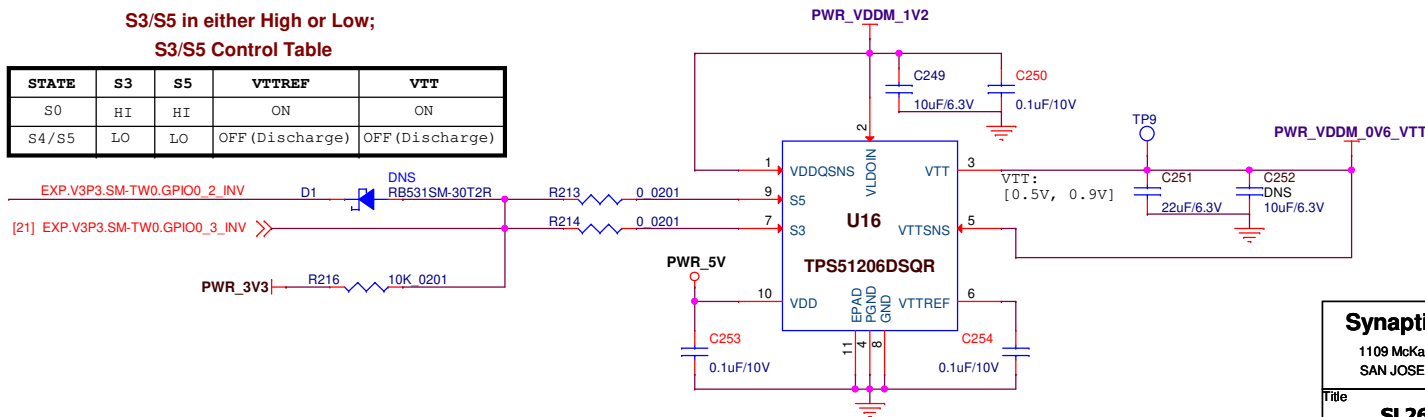


Power-Up Sequence For DDR4 DEVICE

VTT (0.6V) 1.2A Supply for DDR-DEVICES;

S3/S5 in either High or Low;
S3/S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)



Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131



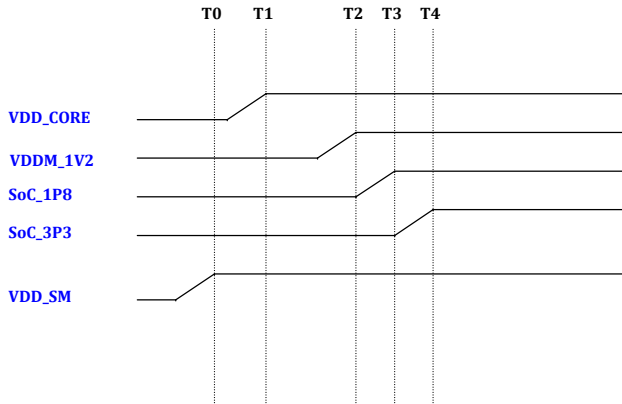
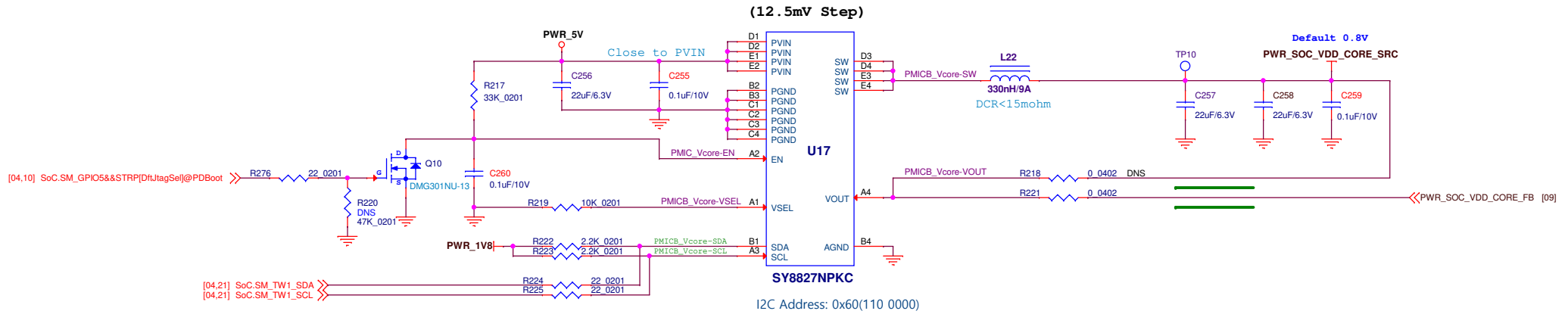
Title
SL2610 CORE MODULE

Size
Document Number
SC950-C01132-01

Date: Thursday, October 23, 2025 Sheet 18 of 21

Rev
B

0.8V/6A for SL2610 SOC_VDD_CORE



SL2610 Recommended Power Sequence

Synaptics, Inc.
1109 McKay Dr.
SAN JOSE, CA 95131

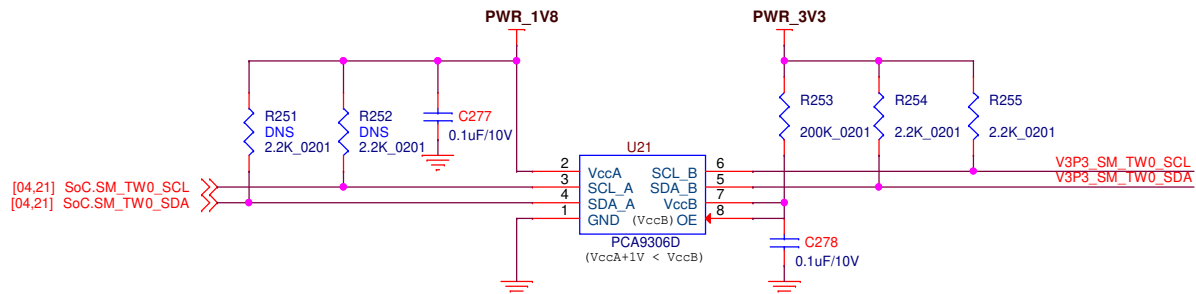
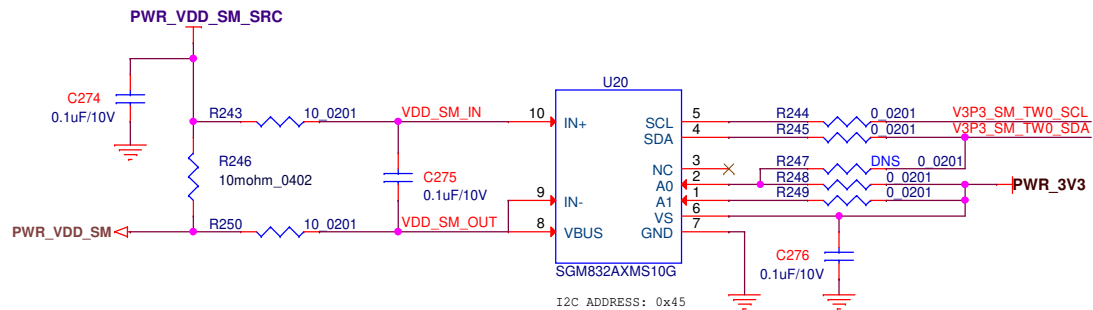
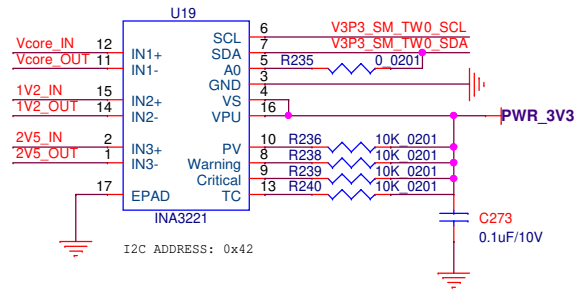
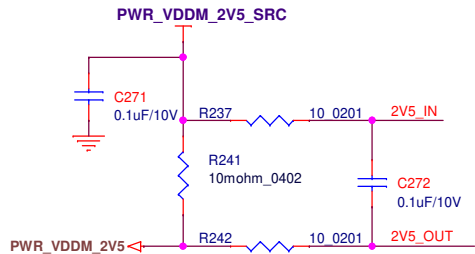
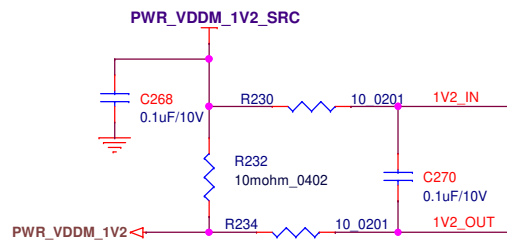
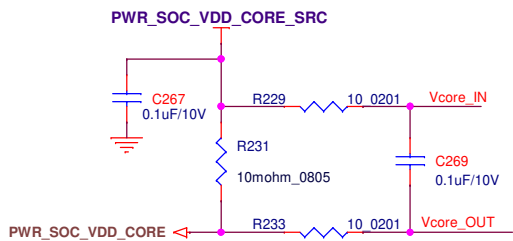
synaptics

SL2610 CORE MODULE

Document Number
SC950-C01132-01

Rev
B

Date: Thursday, October 23, 2025 Sheet 19 of 21



Synaptics, Inc.

1109 McKay Dr.
SAN JOSE, CA 95131



SL2610 CORE MODULE

Size Document Number
SC950-C01132-01

Rev
B

Date: Thursday, October 23, 2025 Sheet 20 of 21

